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December 5, 1997

Attorney Docket No.: 06666/013001

Box Reissue Application
Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a Reissue Patent Application of:

U.S. Patent No.:	5,473,526
Issued:	December 5, 1995
Applicant:	LARS SVENSSON, WILLIAM C. ATHAS, AND JEFFREY G. KOLLER
Title:	SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53, without signatures. Applicants will later file a reissue declaration with offer to surrender original patent, upon receiving a notice of missing parts:

	Pages
Specification	7
Claims	7
Abstract	1
Declaration	[To Be Filed At A Later Date]
Drawing(s)	4

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Date of Deposit December 5, 1997
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Amy N. Hunt

Enclosures:

- Postcard.

Basic filing fee	$ 395.00
Total claims in excess of 20 times $11.00	286.00
Independent claims in excess of 3 times $41.00	287.00
Multiple dependent claims	0.00
Total filing fee:	$ 968.00

Under 37 CFR §1.53(d), no filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney docket number shown above. A duplicate copy of this transmittal letter is attached.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

Mark D. Wiegaek, Reg. No. 37,966

For Scott C. Harris
Reg. No. 32,030

Enclosures
47200

*PATENT
ATTORNEY DOCKET NO. 06666/013001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Svensson, *et al.*
Title : **SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE**
Application for Reissue of U.S. Patent No. 5,473,526
Issued : December 5, 1995
Reissue
Serial No.: 08/986,327
Reissue
Filed : 12/5/97

Asst. Commissioner of Patents and Trademarks
Washington, DC 20231

CONSENT OF ASSIGNEE

The undersigned, whose title is supplied below, is empowered to act on behalf of the assignee.

The undersigned, acting on behalf of the assignee, hereby offers to surrender the above-identified Letters Patent, and consents to the accompanying reissue application. The undersigned further requests that Letters Patent be reissued to it for the same invention upon the foregoing amended application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

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Duncan C. Clark

DUNCAN C. CLARK

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Date: 7/2/98

Dennis F. Dougherty

Name: Dennis F. Dougherty
Title: Sr. Vice President, Administration

46834

*PATENT
ATTORNEY DOCKET NO. 06666/013001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Svensson, *et al.*
Title : **SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE**
Application for Reissue of U.S. Patent No. 5,473,526
Issued : December 5, 1995
Reissue Serial No.: 08/986,327
Reissue Filed : 12/5/97

Commissioner of Patents and Trademarks
Washington, DC 20231

STATEMENT UNDER 3.73(b)

Under 37 CFR §3.73(b), the University of Southern California, a corporation of California, certifies that it is the assignee of the entire right, title and interest in the patent identified above by virtue of an assignment from the inventors. The assignment was recorded in the Patent and Trademark Office at Reel 0744, Frame 0586, on June 17, 1994.

The undersigned has reviewed all the documents in the chain of title of the patent, and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

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Duncan L. Clark

DUNCAN L. CLARK

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Date: 7/2/98

Name: Dennis F. Dougherty
Title: Sr. Vice President, Administration

46834.LJ1

SECTOR 4

PATENT
ATTORNEY DOCKET NO. 06666/013001

#3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Svensson, et al. Art Unit: 2111
Serial No.: 08/986,327 Examiner:
Filed : December 5, 1997
Title : SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

Assistant Commissioner for Patents
Washington, DC 20231

Attention: Box Missing Parts

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION

Sir:

Responsive to the Notice to File Missing Parts of Application under 37 CFR 1.27 mailed February 9, 1998 (a copy of which is enclosed), Applicants as a small entity submit herewith the following:

Payment of the basic filing fee of $395.00.

Payment of the additional claims fees of $286.00.

Payment of the additional independent claims fees of $328.00.

A Declaration and Power of Attorney for Reissue Application in compliance with 37 CFR 1.171.

Consent of Assignee in compliance with 37 CFR 1.172.

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Duncan G. Clark

DUNCAN G. CLARK

Assignee's Statement in compliance with 37 CFR 3.73(b).

Payment of the surcharge of $65.00 for late filing of the basic filing fee/declaration.

Payment of the extension fee of $475.00 and Petition for Extension of Time.

A Verified Statement (Declaration) Claiming Small Entity Status (37 CFR 1.9(f) and 1.27(d)) - NONPROFIT ORGANIZATION.

A check in the amount of $1,549.00 is attached.

It is understood that this perfects the application and no additional papers or filing fees are required. If there are any other charges, or any credits, please apply them to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 8, 1998

FOR Scott C. Harris, Reg. No. 37,966
Scott C. Harris
Reg. No. 32,030

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61490.LJ1

APPLICATION

FOR REISSUE OF

UNITED STATES LETTERS PATENT

NUMBER 5,473,526

TITLE: SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

APPLICANT: LARS SVENSSON, WILLIAM C. ATHAS AND JEFFREY G. KOLLER

"EXPRESS MAIL" Mailing Label Number EM367761948US
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Amy M. Hunt

SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electronic circuits and systems. More specifically, the present invention relates to power dissipation in electronic circuits and systems.

2. Description of the Related Art

Power dissipation of electronic circuitry is an important design consideration for many applications. Power dissipation provides a measure of the efficiency of the system. The efficiency of the system impacts the design of the power supply for the system. That is, low efficiency leads to higher costs due to the waste of energy and the need for larger power supplies.

For battery powered systems, power dissipation limits battery life. This necessitates larger batteries which increases the cost and weight of the system while limiting the applicability thereof. As an example, consider coronary pacemakers where power dissipation is a critical concern due to the difficultly of accessing the battery for replacement and the cost and inconvenience associated with the use of larger batteries.

In addition, the dissipated energy is released in the form of heat. Accordingly, systems which exhibit considerable power dissipation often require measures such as heat sinks to protect or cool system components from the heat created by the circuit. The use of heat sinks and the like adds to the cost, size and weight of the system and thereby limits the utility of same.

For the CMOS (complementary-metal-oxide semiconductor) based system, used widely in the design of computers, digital logic circuits and the like, capacitive effects are primarily responsible for the dissipation of power. Such capacitive effects arise due to junction capacitances within semiconductor devices, interlead capacitances between lines connecting the circuit to external devices and the capacitance of a load.

In accordance with conventional teachings, power dissipation is directly related to the operating frequency (f), the capacitance (C) and the square of the voltage (V^2) applied to the capacitive element.

In addition to the elimination of unnecessary capacitances and the reduction of the switching frequency to the lowest value that supports the functional specification of the circuit, most prior approaches to the problem have focused on reducing the voltage applied to the capacitive elements. However, in addition to costly interfacing issues, attempts to lower the voltage of digital processors and the like have been limited by the fact that the trend is to higher processing speeds which cannot be attained at arbitrarily low operating voltages.

Thus, there is an ongoing need in the art for a system and technique for minimizing the power dissipated by a digital system.

SUMMARY OF THE INVENTION

The need in the art is addressed by the present invention which, in a most general sense, provides a system and method for efficiently charging and discharging a capacitive load from a single voltage source. The inventive system

includes a first switch for selectively connecting the voltage source to the load and a second switch for selectively providing a short across the load as may be common in the art. A particularly novel aspect of the invention resides in the provision of plural capacitive elements and a switching mechanism for selectively connecting each of the capacitive elements to the load whereby the load is gradually charged or discharged.

In the illustrative embodiment, the switching mechanism includes a set of switches for selectively connecting each of the capacitive elements to the capacitive load and a switch control mechanism for selectively activating the switches.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified representation of a conventional driver for a capacitive load.

FIG. **2** shows a system for charging the load capacitance by several steps and thereby reducing power dissipation.

FIG. **3** is a simplified schematic of a preferred embodiment of the circuit of the present invention for reducing the power dissipation of a capacitive load.

FIG. **4** is a diagram showing the control circuit of the driver constructed in accordance with the teachings of the present invention.

FIG. **5** is a timing diagram which illustrates the operation of the driver of the present invention.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof.

Most of the power dissipation in digital CMOS circuits is due to repeated charging and discharging of capacitive loads including those internal to the circuit and those associated with the output signals.

FIG. **1** is a simplified representation of a conventional driver for a capacitive load. The load C_L represents the capacitance of a load and the interlead capacitance of the lines connecting the driver **10'** to the load **12'**. The load **12'** is charged to the supply voltage V by connecting the load **12'** to the power rail via a first switch **14'**. In practice, the switch **14'** may be a metal-oxide semiconductor field-effect transistor (MOSFET) which has a nominal "on" resistance. When the switch **14'** is closed, a charge CV passes through the resistance of the switch **14'**. The voltage drop across the resistance varies from an initial value of V to a final value of zero, so the average voltage drop V' traversed by the charge is V/2, if the capacitance is linear. The energy dissipated is:

$$E_{conv}=QV'=CV\,(V/2)=CV^2/2 \qquad [1]$$

A similar argument applies to the discharge process, so a complete conventional charge-discharge cycle dissipates all the energy provided by the power supply, $QV=CV^2$.

In accordance with the present teachings, power dissipation is reduced by charging the capacitance of the load C_L in several steps. This is illustrated in FIG. 2.

FIG. 2 shows a system **10** for charging the load capacitance by several steps and thereby reducing power dissipation. Here, a bank of supply voltages V_1 to V_N are used to charge the load 12. The voltages of the supplies are evenly distributed between ground and V_N so that the voltage difference between any two adjacent supplies is the same. Each of the voltages is selectively applied to the load **12** by N switches including the first switch **14** and N−1 additional switches. Between charge cycles, switch **0** is closed. To charge the load, switch **0** is opened and the supplies V_1 through V_N are connected to the load in succession by selectively closing the switches, that is, by momentarily closing switch 1, opening switch **1**, momentarily closing switch **2** etc. To discharge the load, the supplies V_{N-1} through V_1 are switched in in reverse order. Then switch **0** is closed connecting the output to ground.

If N steps are used, the dissipation per step is again given by the transferred charge and the average voltage drop across the switch resistance:

$$E_{step}=QV=(CV/N)\,(V/2N)=CV2/2N^2 \qquad [2]$$

To charge the capacitance all the way to the supply voltage V, N steps are used, so the total energy dissipation is:

$$\begin{aligned} E_{stepwise} &= N*E_{step} \qquad [3]\\ &= N*CV^2/2N^2\\ &= CV^2/2N\\ &= E_{conv}/N \end{aligned}$$

Again, a full charge-discharge cycle will cause twice the dissipation of the charging only. Thus, according to this simplified analysis, charging by several steps reduces the energy dissipation per charge-discharge cycle and thereby the total power dissipation, by a factor of N.

The multiple supply voltages of FIG. 2 may be generated with a battery stack. For equipment not powered by batteries or when the desired voltage increment is not a multiple of the battery cell voltage, a power supply unit would seemingly have to generate these multiple supply voltages with an associated cost in expense, complexity and power dissipation.

FIG. 3 is a simplified schematic of a preferred embodiment of the circuit of the present invention for reducing the power dissipation of a capacitive load. The circuit **100** is essentially identical to that of FIG. 2 with the exception that the supplies V_1−V_{N-1} are replaced with a corresponding number of capacitors C_T **18** which will be referred to as "tank" capacitors. Each tank capacitor C_T has a capacitance which is much, much larger (e.g. an order of magnitude) than the load capacitance C_L. Switch operations are sequenced by a control circuit **20**.

FIG. 4 is a diagram showing the control circuit **20** interconnected to plural MOSFET switches for an N=6 implementation of the driver constructed in accordance with the teachings of the present invention. In FIG. 4, the tank capacitors **18** are eliminated for simplicity. The control signals may be provided by the circuit **20** or may be supplied by a host microprocessor. The control circuit **20** may be implemented in several configurations. For example, the control circuit may be implemented with a microprocessor or with a shift register and a counter. In the alternative, a latch **22** and input and output logic circuits **24** and **26**, respectively, may be used as shown in FIG. 4. The input and

output logic circuits may be designed by a computer aided logic design program of which several are currently available. If a computer aided logic design program is used, the desired outputs would be specified in response to the expected input signals. The program would then design the logic circuits.

Timing signals are provided by a system clock (not shown) through the latch **22**. In practice, the clock rate should be at least (N+1) times the output signal rate. In the preferred embodiment, switches **0–4** are implemented with n-channel MOSFET devices. Switches **5** and **6** are implemented with p-channel devices.

FIG. **5** is a timing diagram which illustrates the operation of the driver **100** of the present invention. In FIG. **5**(*a*), the clock pulses are shown. The input signal is shown in FIG. **5**(*b*). FIGS. **5**(*c*)–(*i*) show the controls for switch **0–6** and FIG. **5**(*j*) shows the output at the load C_L.

The operation of the circuits of FIGS. **3** and **4** is essentially the same as that of FIG. **2**. That is, in the initial standby condition switch **0** is closed and there is no charge on any of the capacitors in the system. Next, when an input pulse is to be transferred to the load, switch **0** is opened and switch **1** is closed. Since there is no charge on the load, C_L nor on any of the tank capacitors C_T, there will be no charge transfer through any of the switches as each is closed, in turn, momentarily. When the first switch **14** is closed, a charge is applied to the load **12**.

On the trailing edge of input pulse, a discharge cycle is initiated by when the switches are momentarily closed in reverse order. Thus, switch N is opened and switch N–1 is closed. Then switch N–1 is opened and switch N–2 is closed and etc. On the closure of switch N–1, the associated tank capacitor will receive most of the charge on the load capacitance. Each capacitor down the line will receive a lower charge than the immediately proceeding capacitor. After switch **1** opens, switch **0** closes to complete the cycle dumping the remaining charge on the load C_L to ground. Thus, over several cycles the tank capacitors will approach their steady state voltages, for example, the (N–1) th through 1st tank capacitors may have charges of say 5, 4, 3, 2 and 1 volts respectively. Then, at the beginning of the next cycle, on the closure of the first switch, the voltage on the first tank capacitor is applied to the load, then the voltage on the second capacitor is applied to the load and so on. Thus, in the example, first 1 volt is applied to the load, then 2 volts, then three volts and etc. As a result, the voltage on the load will gradually increase as shown in FIG. **5**(*j*).

The circuits of FIG. **3** and **4** will provide the same power dissipation reduction as that of FIG. **2**, but without multiply supply lines and without complicating the power supply. This is illustrated by the following analysis. Assume that each tank capacitor C_T is charged to the voltage of the corresponding supply of FIG. **2**, and that the load capacitance C_L is discharged. The load capacitance is charged by closing and opening switches **1** through N in succession. Each tank capacitor (and the power supply) delivers a charge given by:

$$q=C_L V/N \qquad [4]$$

Since the tank capacitors are much larger than the load, the tank voltages do not change significantly, so the dissipation in the switches will be the same as for the case in FIG. **2**, where the supply voltages are constant. To discharge the load capacitance, switches N–1 through **0** are closed and opened in succession. During the discharge, each tank capacitor receives a charge of the same size as that delivered during charge phase, and an equally sized charge is dumped

to ground via switch 0. Over the full charge-discharge cycle, only the power supply injects any charge into the circuit. No net charge is drawn from any tank capacitor, so the tank voltages do not change.

The voltages of the tank capacitor bank are self-stabilizing. To appreciate this, assume that the voltage of one of the tank capacitors is slightly higher than it should be. Then, the charge delivered by this tank capacitor during the charging of the load will be somewhat larger than that given by equation [4], since the "step" from the voltage below is now slightly larger. During the discharge phase, the step from the voltage above is slightly smaller and the charge received is therefore smaller as well. Therefore, over the full cycle, a net decrease of the charge on the storage capacitor occurs, which causes a decrease in the capacitor voltage. The initial deviance is automatically counteracted.

Even if the tank capacitor voltages differ from the "correct" values, the circuit will work logically correctly, since each charging (discharging) cycle ends by connecting the load to he supply rail (ground). Voltage deviations simply bring higher dissipation. This happens during start-up, before the tank voltages have had time to converge to the even distribution between the supply voltage and ground.

The implementation cost of a driver such as that shown in FIG. 3 is determined by the tank capacitors, the switches, the mechanism controlling the switches, and the interconnections of same. Note that all extra interconnections are local. As for the conventional case, only one connection to the power supply is needed. Also, several drivers may share the same capacitor bank and part of the control mechanism.

The problem of maintaining the appropriate voltages on the tank capacitors is obviated by the fact that the capacitor voltages will converge automatically to the desired voltages. No additional circuitry is required. Only one supply line must be routed to the chip and the power supply need not be any more complicated than a conventional supply. In practice, the tank capacitors would be located off-chip.

For a CMOS implementation, the following design procedure may be followed to provide a driver configuration which exhibits minimal power dissipation.

Equation [3] indicates that dissipation decreases monotonically with increasing N. The number N cannot, however, be usefully made arbitrarily large because each step requires that a switch be turned on and off, which itself causes dissipation. Also, the energy used to drive each switch depends on the width of the device, which should be just enough to allow the charging to complete before the next step commences. Thus, for a given total allowable charging time "T", there is an optimal number of steps and a set of optimal device sizes which lead to minimal total dissipation determined as follows.

Again, consider the circuit in FIG. 3 and assume the gates of the switch devices are driven conventionally. The load is charged and discharged once; the energy needed to drive the gates of the switch devices is:

$$E_{sw} = \left(\sum_{i=1}^{N} C_i + \sum_{i=0}^{N-1} C_i \right) V^2 \qquad [5]$$

Allot each step one Nth of the total charging time T. Then:

$$T/N = mR_iC_i \qquad [6]$$

Here, m is the number of RC time constants spent waiting for each charging step to complete. From equation [6], it is evident that all the switch devices should have equal on-resistance: $R_i = R_{sw}$. Decreasing the on-resistance of device i

by increasing the width means increasing the gate capacitance:

$$R_i C_i = \rho_i \quad [7]$$

ρ_i is a quality measure of the switch. It varies with i, since the bulk-to-channel and gate-to-channel voltages are different for different switches. Combining equations [5], [6], and [7] yields:

$$E_{sw} = \frac{Nm}{T}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i \right) C_L V^2 \quad [8]$$

Introducing $\bar{\rho}$, a weighted average of ρ_i for the different switches:

$$\bar{\rho} = \frac{1}{2N}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i \right) \quad [9]$$

If N is sufficiently large, $\bar{\rho}$ is close to the unweighed average of ρ over the entire voltage range. Combining equations [3], [8] and [9] yields the following expression for the total energy dissipation:

$$E_{tot} = \left(\frac{1}{N} + 2N^2 m \frac{\bar{\rho}}{T} \right) C_L V^2 \quad [10]$$

The number N that minimizes E_{tot} is given by:

$$N_{opt} = \sqrt[3]{\frac{T}{4m\bar{\rho}}} \quad [11]$$

The corresponding energy dissipation is:

$$E_{opt} = \frac{3}{2}\sqrt[3]{\frac{4m\bar{\rho}}{T}}\, C_L V^2 \quad [12]$$

It remains to select the value for m. If it is chosen too small, there will still be a significant voltage across a switch when the next switch is to close. Hence, there is an increase in the average voltage across each switch and therefore a dissipation increase (the first term in equation [10] is changed slightly). If on the other hand, m is chosen unnecessarily large, time is wasted that could have been used to increase the number of steps. Thus, in general, optimization methods for the value of m vary according to the application, however, one skilled in the art will be able to select a suitable value for m using conventional teachings (e.g., a simulation program).

By using the number of stages given by equation [10], the designer can minimize the power dissipation of the driver. The minimum is rather shallow, however, so a lower N (as would most often be dictated by practical considerations) will still give a considerable improvement over the conventional case; N=2 already gives almost 50% reduction. Once N and m have been selected, the on-resistance of each switch is given by equation [6]. The corresponding gate capacitance, and thereby the width of the device, is given by equation [7]. The values of ρ for a certain process can be found by circuit simulation or by measuring the on-resistances of test devices of known widths.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications applications and embodiments within the scope

thereof. For example, the switches may be closed in some other sequence as may be appropriate for a given application without departing from the scope of the present invention. In addition, alternative circuit topologies for the network of tank capacitors and switches may be appropriate. The second terminal of the load may be connected to a potentially variable) voltage other than ground.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

What is claimed is:

1. A system for efficiently charging and discharging a capacitive load from a single voltage source of a first potential consisting of:

a first switch for selectively charging the load;

a second switch for selectively discharging the load;

plural capacitive elements; and

switch means for selectively connecting each of the capacitive elements to the capacitive load to gradually charge or discharge the capacitive load.

2. The invention of claim **1** wherein said switch means includes plural third switches connected between said capacitive elements and said load.

3. The invention of claim **2** wherein said switch means includes means for selectively activating the first, second and third switches.

4. The invention of claim **3** wherein the capacitive load has a first terminal connected to the first switch and a second terminal connected to a source of a second potential.

5. The invention of claim **4** wherein the second switch has a first terminal connected to the first terminal of the load and a second terminal connected to said source of a second potential.

6. The invention of claim 5 wherein each of the third switches has a first terminal connected to the first terminal of the load and a second terminal connected to a first terminal of an associated one of the plural capacitive elements.

7. The invention of claim 6 wherein the means for selectively activating the first, second and third switches includes a finite state machine.

8. The invention of claim 7 wherein the finite state machine is designed to receive a clock signal and an input signal and provide selective activation signals for the first, second and third switches in response thereto.

9. The invention of claim 8 wherein a second terminal of each of the plural capacitive elements is connected to said source of a second potential.

10. The invention of claim 9 wherein each of the capacitive elements has a capacitance which is at least an order of magnitude greater than the capacitance of the load.

11. A method for efficiently charging and discharging a capacitive load from a single voltage source including the steps of:

providing a first switch for selectively connecting the voltage source to the load;

providing a second switch for selectively providing a short across the load;

providing plural capacitive elements;

providing plural third switches for selectively connecting each of the capacitive elements to the capacitive load; and

selectively activating the first, second and third switches to gradually charge or discharge the capacitive load.

12. A system for charging and discharging a capacitive load, comprising:

a first switch to charge the load;

a second switch to discharge the load;

a charge storage element; and

a switch assembly to connect the charge storage element to the capacitive load to gradually charge or discharge the capacitive load.

13. The system of claim 12 wherein said switch assembly includes a third switch connected between said charge storage element and said capacitive load.

14. The system of claim 13 wherein said switch assembly includes means for selectively activating the first, second and third switches.

15. The system of claim 14 wherein the capacitive load has a first terminal connected to the first switch and a second terminal connected to a source of a potential.

16. The system of claim 15 wherein the second switch has a first terminal connected to the first terminal of the capacitive load and a second terminal connected to said source of a potential.

17. The system of claim 16 wherein said third switch has a first terminal connected to the first terminal of the capacitive load and a second terminal connected to a first terminal of said charge storage element.

18. The system of claim 12 wherein said switch assembly includes a finite state machine.

19. The system of claim 13 wherein the finite state machine is designed to receive a clock signal and an input signal and provide selective activation signals for the first, second and third switches in response thereto.

20. The system of claim 19 wherein a second terminal of said charge storage element is connected to said source of a potential.

21. The system of claim 20 wherein a capacitance of said charge storage element is at least an order of magnitude greater than a capacitance of the capacitive load.

22. The system of claim 12, further comprising:

at least two charge storage elements,

such that said switch assembly selectively connects each of said at least two charge storage elements to the capacitive load.

23. The system of claim 12, wherein said charge storage element is a capacitor.

24. The system of claim 12, wherein said switch assembly includes a control circuit.

25. The system of claim 22, wherein said switch assembly includes a control circuit employing a plurality of MOSFETS.

26. A system for charging and discharging a capacitive load from a voltage source comprising:

a first switch to charge the load;

a second switch to discharge the load;

a charge storage element; and

a switch assembly to connect the charge storage element to the capacitive load to charge or discharge the capacitive load in a plurality of steps.

27. A method for charging and discharging a capacitive load from a voltage source comprising the steps of:

charging said capacitive load with said voltage source; and

discharging said capacitive load by connecting said capacitive load through a switch assembly to at least one charge storage element.

28. The method of claim 27, further comprising:

operating said switch assembly to sequentially discharge said capacitive load through at least two charge storage elements.

29. A method for charging and discharging a capacitive load from a voltage source comprising:

charging said capacitive load with said voltage source; and

temporarily storing the charge from said capacitive load for use in a subsequent charging step.

30. A system for charging and discharging a load with a source comprising:

a first lead to charge the load;

a second lead to discharge the load;

a charge storage element; and

a switch to selectively connect the charge storage element to the load.

31. A system for at least one of charging and discharging a capacitive load comprising:

a charge storage device; and

a first switching device operable to selectively couple the charge storage device to the capacitive load during at least one of a charging and a discharging of the capacitive load.

32. The system of claim 31, wherein the first switching device is operable to selectively couple the charge storage device to the capacitive load during both the charging and the discharging of the capacitive load.

33. The system of claim 31, wherein the charge storage device includes a capacitor.

34. The system of claim 33, wherein a capacitance of the capacitor is greater than a capacitance of the capacitive load.

35. The system of claim 31, wherein the first switching device includes a MOSFET.

36. The system of claim 31, wherein the selective coupling of the charge storage device to the capacitive load causes at least one of the charging and the discharging of the capacitive load to occur in a plurality of steps.

37. The system of claim 31, further comprising:

a second switching device operable to selectively couple the capacitive load to a voltage source; and

a third switching device operable to selectively provide a short across the capacitive load.

38. A system for at least one of charging and discharging a capacitive load comprising:

a plurality of charge storage devices; and

a first switching device operable to selectively couple the plurality of charge storage devices to the capacitive load during at least one of a charging and a discharging of the capacitive load.

39. The system of claim 38, wherein the first switching device includes a plurality of MOSFETs.

40. The system of claim 38, wherein the first switching device is operable to selectively couple the plurality of charge storage devices to the capacitive load during both the charging and the discharging of the capacitive load.

41. The system of claim 38, wherein each of the plurality of charge storage devices includes a capacitor.

42. The system of claim 41, wherein a capacitance of the capacitor is greater than a capacitance of the capacitive load.

43. The system of claim 38, wherein the selective coupling of the plurality of charge storage devices to the capacitive load causes at least one of the charging and the discharging of the capacitive load to occur in a plurality of steps.

44. The system of claim 38, comprising:

a second switching device operable to selectively couple the capacitive load to a voltage source; and

a third switching device operable to selectively provide a short across the capacitive load.

45. A method for at least one of charging and discharging a capacitive load comprising the step of:

selectively coupling a charge storage device to the capacitive load to cause at least one of the charging and the discharging of the capacitive load to occur in a plurality of steps.

46. A method for charging and discharging a capacitive load comprising the steps of:

charging the capacitive load;

discharging the capacitive load; and

storing at least a portion of a charge discharged during the discharging step for use in a subsequent charging step.

ABSTRACT

A system and method for efficiently charging and discharging a capacitive load from a single voltage source. The system includes a first switch for selectively connecting the voltage source to the load and a second switch for selectively providing a short across the load as may be common in the art. A particularly novel aspect of the invention resides in the provision of plural capacitive elements and a switching mechanism for selectively connecting each of the capacitive elements to the load whereby the load is gradually charged or discharged. In the illustrative embodiment, the switching mechanism includes a set of switches for selectively connecting each of the capacitive elements to the capacitive load and a switch control mechanism for selectively activating the switches.

FIG. 1 PRIOR ART

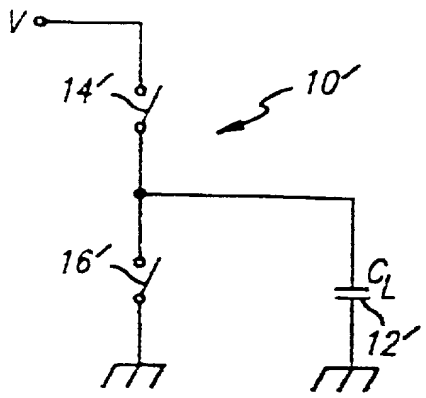


FIG. 2 PRIOR ART

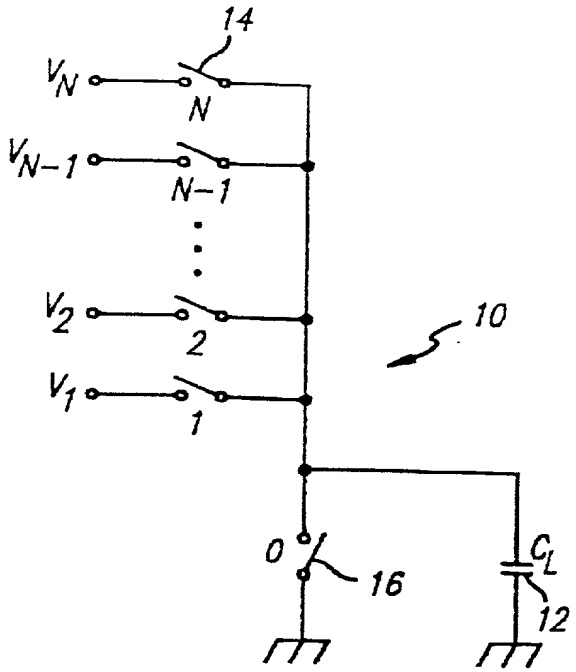
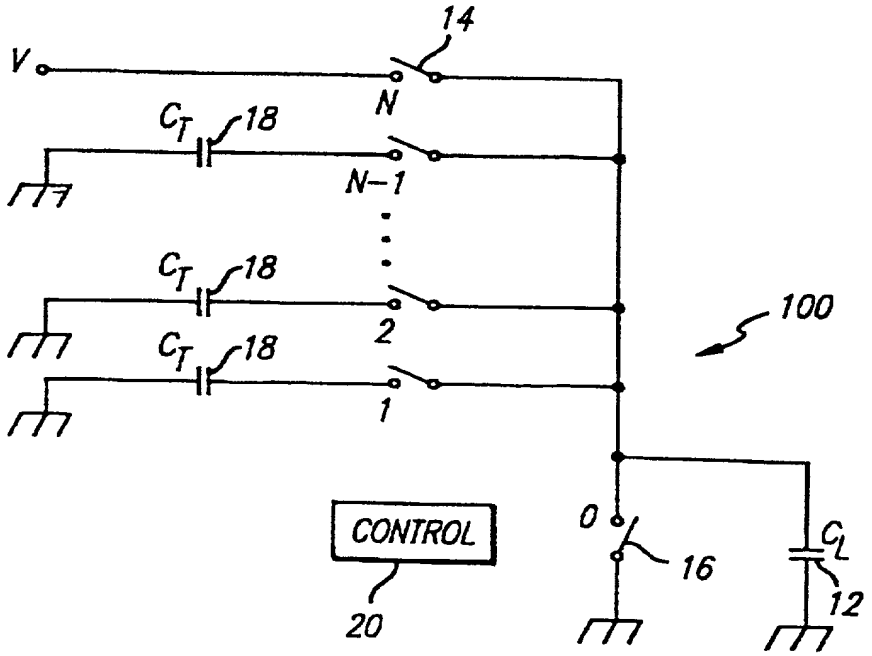


FIG. 3



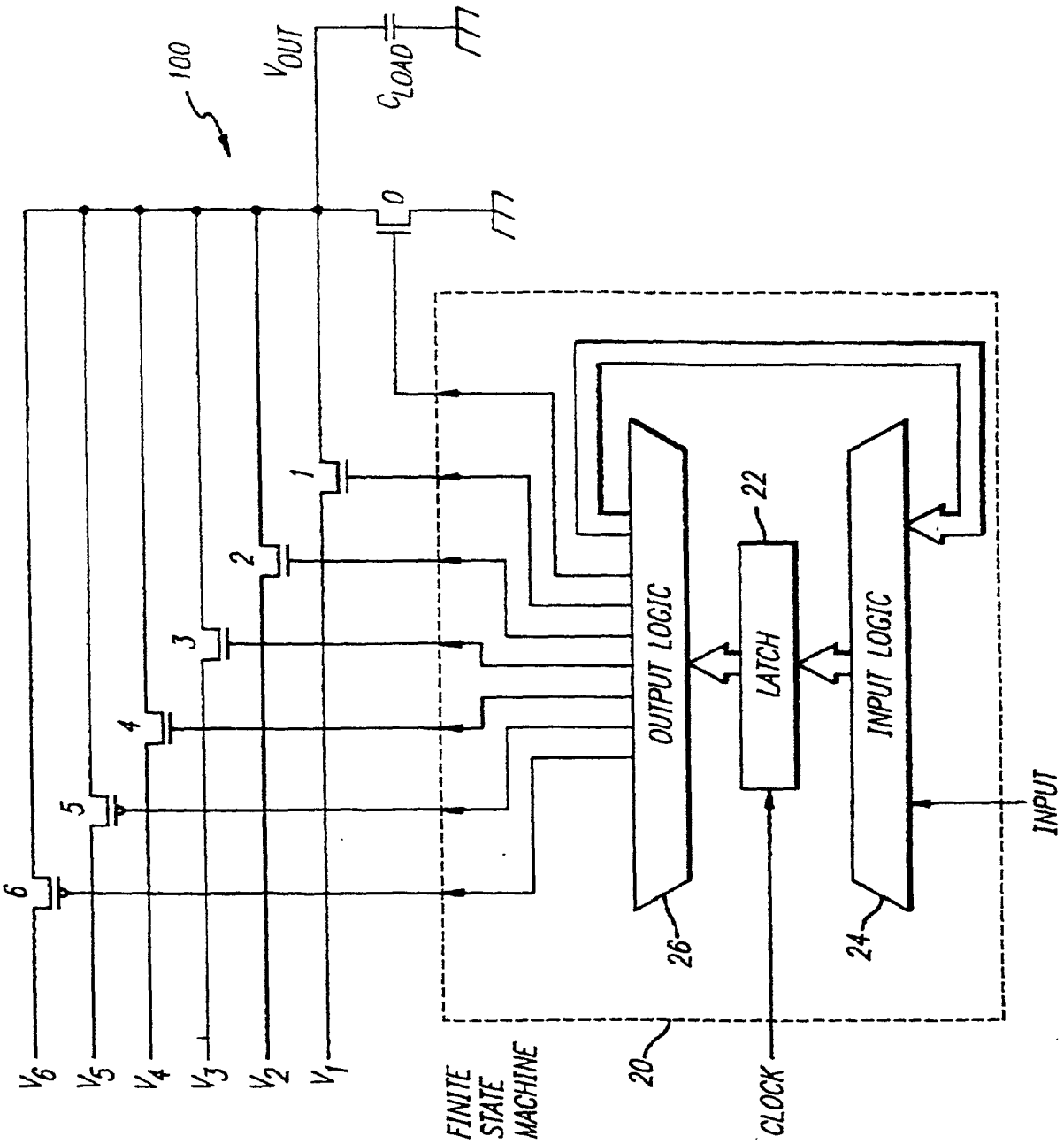

100
V_{OUT}
C_{LOAD}
0
1
2
3
4
5
6
V_6
V_5
V_4
V_3
V_2
V_1
OUTPUT LOGIC
LATCH
INPUT LOGIC
22
26
24
INPUT
FINITE STATE MACHINE
20
CLOCK

FIG. 4

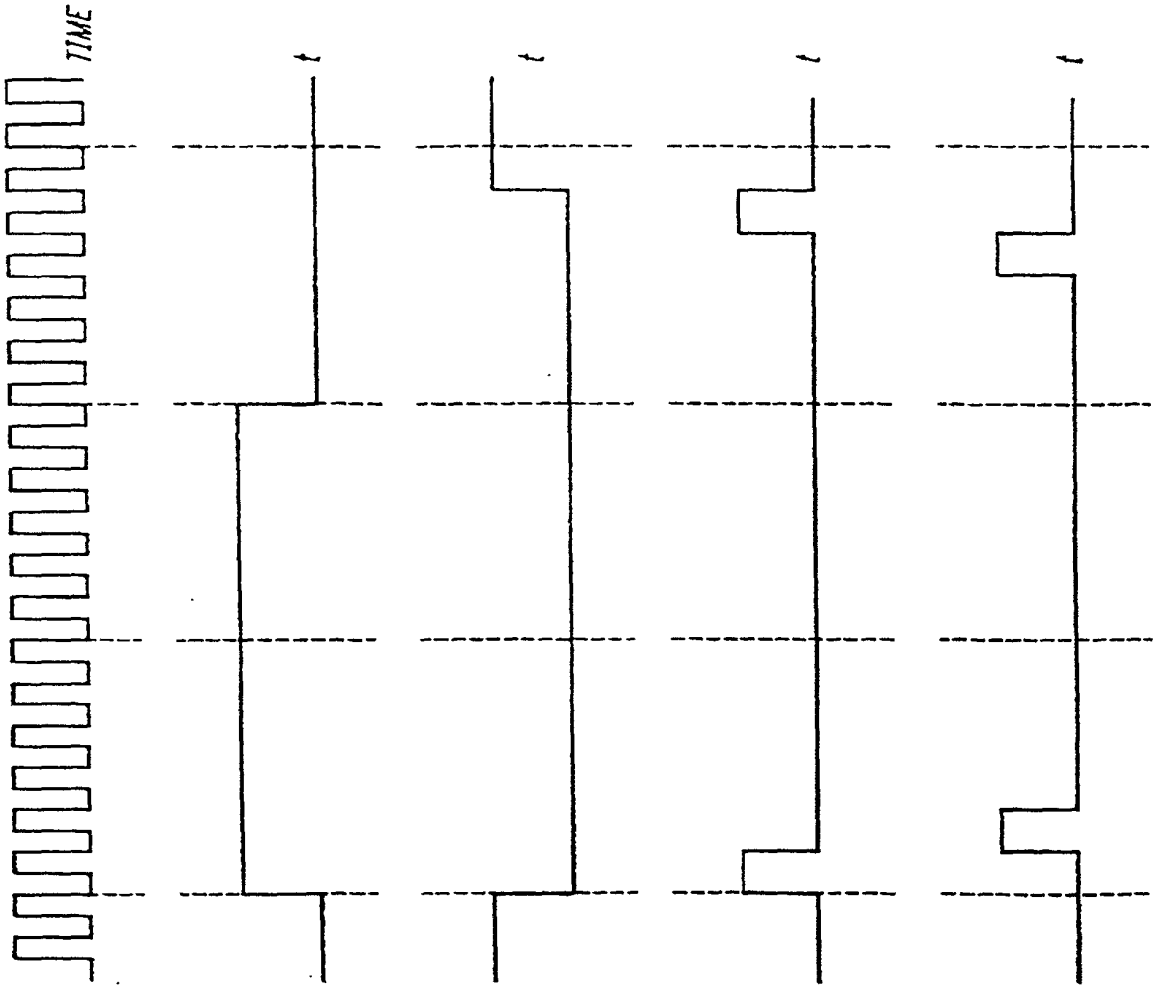


FIG. 5(a) CLOCK

FIG. 5(b) INPUT

FIG. 5(c) SWITCH #0 CONTROL

FIG. 5(d) SWITCH #1 CONTROL

FIG. 5(e) SWITCH #2 CONTROL

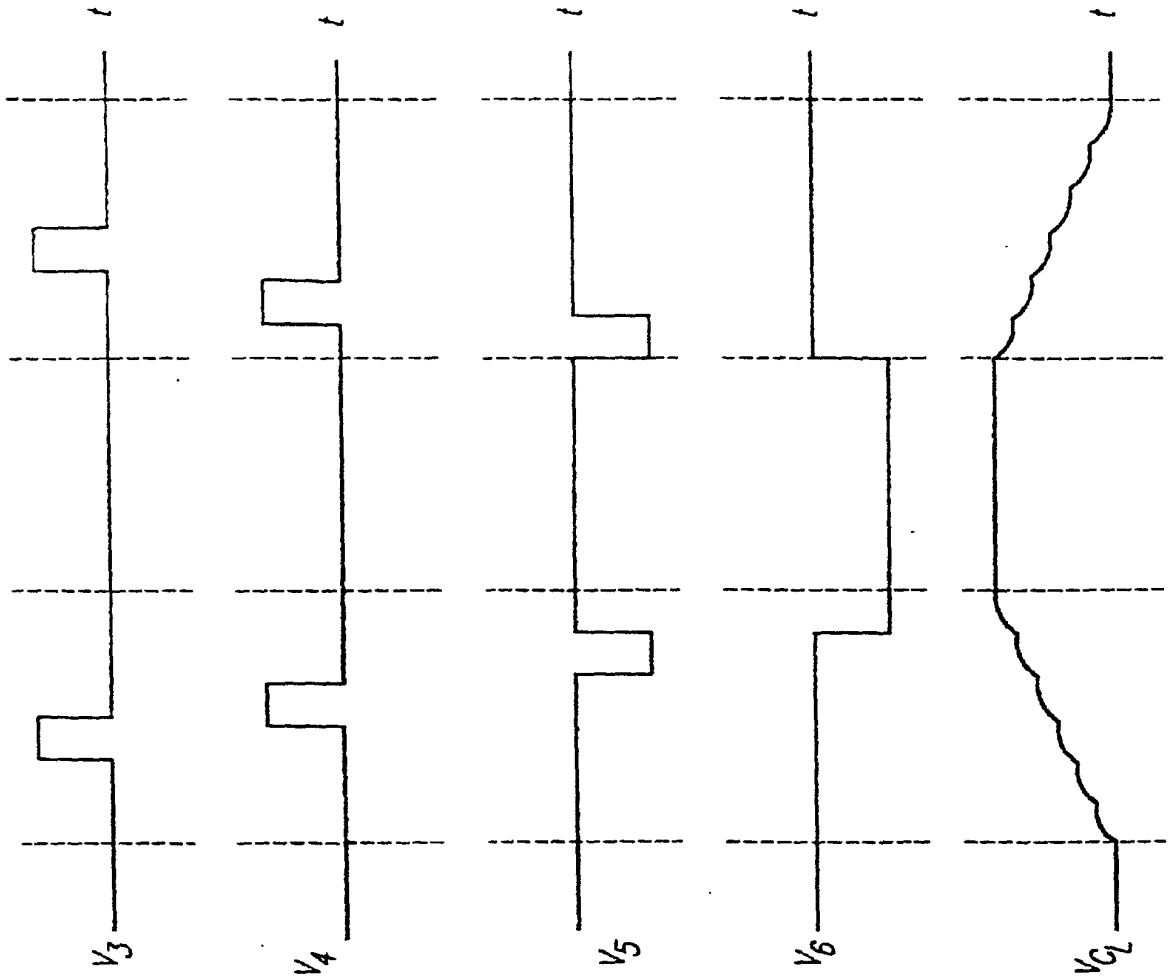


FIG. 5(f)

FIG. 5(g)

FIG. 5(h)

FIG. 5(i)

FIG. 5(j)

#3

*PATENT
ATTORNEY DOCKET NO. 06666/013001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Svensson, *et al.*
Title : **SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE**
Application for Reissue of U.S. Patent No. 5473,526
Issued : December 5, 1995
Reissue
Serial No.: 08/986,327
Reissue
Filed : 12/5/97

Commissioner of Patents and Trademarks
Washington, DC 20231

Declaration and Power of Attorney for Reissue Application
Pursuant to 37 C.F.R. §1.171 et seq.

Sir:

We, Lars Svensson, William C. Athas, and Jeffrey G. Koller, hereby declare that our residences, Post Office addresses and citizenships are as stated below next to our names, and we believe we are the original and joint inventors of the invention entitled SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE described and claimed in the reissue specification filed December 5, 1997 as Application No. 08/986,327 and also described and claimed in our original application No. 08/231,637 filed April 22, 1994, and

"EXPRESS MAIL" Mailing Label Number EM320640788US
Date of Deposit 7-8-98
I hereby certify under 37 CFR 1.10 that this correspondence is being deposited with the United States Postal Service as "**Express Mail Post Office To Addressee**" with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Duncan G. Clark

DUNCAN G CLARK

the resulting United States Patent No. 5,473,526, which issued December 5, 1995; and for which invention a reissue patent is solicited; that we have reviewed and understand the contents of that specification, including the claims, as amended by any amendments specifically referred to in this Declaration; that we acknowledge the duty to disclose information of which we are aware and which is material to the examination of the application in accordance with U.S. law and specifically 37 C.F.R. §1.56(a);

That we verily believe that through error, without any deceptive intent, the said patent is partly inoperative or invalid by reason of our claiming less than we had a right to claim.

The error arose during prosecution due to a misunderstanding of the proper scope of our invention commensurate with the prior art. We understand that the misunderstanding occurred as follows.

The application was originally filed with claims 1-11. Applicants and their counsel believed that these claims were patentable over the prior art applied by the Examiner during the prosecution. Thus, no claim amendments were made.

Applicants and their counsel did not appreciate that they were in fact entitled to broader claim coverage. For example, Applicants did not appreciate that the claimed "plural capacitive elements" could be claimed more broadly without running afoul of the prior art.

After U.S. Patent No. 5,473,526 was issued, a licensee of the assignee was examining the issued claims and noticed that certain claim limitations appeared overly restrictive. The licensee proposed broadening changes to the claims. The licensee believed such broader claims were novel over the cited prior art.

After further study, we agreed that such claims were patentable. The error in the original prosecution which rendered the original patent inoperative or invalid was based on misunderstanding the invention and the specific scope of the novel features of the invention.

We therefore believe that U.S. Patent No. 5,473,526 is inoperative or invalid by reason of our claiming less than we had a right to claim in the patent. The new claims which are presented herein make up this deficiency. The errors relied on arose during prosecution, and were found during a post-issuance study of the technology and the '526 patent. The errors arose without deceptive intent.

We, Lars Svensson, William C. Athas and Jeffrey G. Koller, joint inventors for the above-captioned U.S. Letters Patent, which is the subject of the accompanying application for the reissue, hereby agree to surrender the above-captioned U.S. Letters Patent upon the granting of this reissue.

We hereby state that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose all information we know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56(a).

We hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Address all correspondence to Scott C. Harris, Fish & Richardson P.C., 4225 Executive Square, Suite 1400, La Jolla, California 92037.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: [signature] Date: 6/9/98

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Inventor's Signature: _____ Date: _____

Residence Address: _____

Citizen of: U.S.

Post Office Address: _____

Full Name of Inventor: Jeffrey G. KOLLER

Inventor's Signature: _____ Date: _____

Residence Address: _____

Citizen of: U.S.

Post Office Address: _____

imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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ATTORNEY DOCKET NO. 06666/013001

#3

Applicant or Patentee: Svensson, et al.
Serial or Patent No.: 08/986,327
Filed or Issued: 12/5/97
For: SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(d)) - NONPROFIT ORGANIZATION

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

Name of Organization: UNIVERSITY OF SOUTHERN CALIFORNIA
Address of Organization: 3716 South Hope Street, Los Angeles, California 90007-4344
Type of Organization:

[X] UNIVERSITY OR OTHER INSTITUTION OF HIGHER EDUCATION
[ ] TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c)(3))
[ ] NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA
(NAME OF STATE:)
(CITATION OF STATUTE:)
[ ] WOULD QUALIFY AS TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c)(3)) IF LOCATED IN THE UNITED STATES OF AMERICA
[ ] WOULD QUALIFY AS NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA IF LOCATED IN THE UNITED STATES OF AMERICA
(NAME OF STATE:)
(CITATION OF STATUTE:)

I hereby declare that the nonprofit organization identified above qualifies as a nonprofit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE OAD FROM A SIGNLE SOURCE by inventor(s) Lars Svensson, William C. Athas, Jeffrey G. Koller described in

[ ] the specification filed herewith.
[X] application serial no. 08/986,327, filed 12/5/97.
[ ] patent no. , issued .

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention.

If the rights held by the nonprofit organization are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Full Name: _____

Address: _____

[ ]INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name: Dennis F. Dougherty
Title: Sr. Vice President, Administration
Address: 3716 South Hope Street, Los Angeles, California 90007-4344
Signature: Dennis D Dougherty **Date:** 7/2/98

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